The ARR (Auto-reload register) sets the TOTAL counter length

The CCR sets when to toggle from high to low

TMR1 ch4 – pwm output to PA11 – have set the ARR value to 1024 to give 10-bit PWM resolution and have set clock divider to 2, which gives exactly 31.25kHz at 64MHz clock frequency.

TMR ch5 – used for adc interrupt triggering – 65535 ‘pulse’ (thanks st for stupid name) gives ~10ms overflow frequency. This requires ‘output compare’ mode. Ch5 only ‘outputs’ internally and not to a specific pin.